UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/928,671	08/13/2001	Dennis M. O'Connor	INTL-0606-US (P11747)	8164

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EXAMINER
VITAL, PIERRE M

ART UNIT	PAPER NUMBER
2188	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No. 09/928,671	Applicant(s) O'CONNOR, DENNIS M.
	Examiner Pierre M. Vital	Art Unit 2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2003*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

    a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1.   This Office Action is in response to applicant's communication filed August 20,

2003 in response to PTO Office Action mailed June 26, 2003. The Applicant's remarks

and amendments to the claims and/or the specification were considered with the results

that follow.

2.   Claims 1-30 have been presented for examination in this application. In response

to the last Office Action, claims 8, 10, 18, 20, 28 and 30 have been amended. No claims

have been canceled or added. As a result, claims 1-30 are now pending in this

application.

3.   The objection to the specification has been withdrawn due to the amendment

filed August 20, 2003.

4.   The objection to claims 8-10, 18-20 and 28-30 has been withdrawn due to the

amendment filed August 20, 2003.

5.   The rejection of claims 1-30 as in the Office Action mailed June 26, 2003 (Paper

No. 2) is respectfully maintained and reiterated below for Applicant's convenience.

Claim Rejections - 35 USC § 102

6.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by
> another filed in the United States before the invention by the applicant for patent or (2) a patent
> granted on an application for patent by another filed in the United States before the invention by the
> applicant for patent, except that an international application filed under the treaty defined in section
> 351(a) shall have the effects for purposes of this subsection of an application filed in the United States
> only if the international application designated the United States and was published under Article 21(2)
> of such treaty in the English language.

7.   Claims 1, 2, 5, 6, 8, 11, 12, 15, 16,18, 21, 22, 25, 26 and 28 are rejected under

35 U.S.C. 102(e) as being anticipated by Arimilli et al. (US6,463,507) hereinafter

"Arimilli".

As per claim 1, Arimilli discloses a method comprising defining a multilevel cache

[*e.g., L1 and L2*; col. 8, lines 19-21] including a core having relatively faster components

[*L1 cache is faster since it is closest to processor core*; col. 8, lines 19-21; col. 9, lines 47-50];

and a region including relatively slower components [*directory of the lower level (L2) cache, L2*

cache is slower than L1 cache; col. 5, line 32; *L1 cache is composed of high-speed components, L2*

cache can store a much larger amount of information and encounters a longer access penalty than the L1

cache; col. 2, lines 34-46]; and managing the core from said region [*upper level cache in the*

core is updated by searching lower level cache directory; col. 5, lines 30-33].

As per claim 2, Arimilli discloses managing the core from a level 2 cache [*upper*

level cache in the core is updated by searching lower level (L2) cache directory; col. 5, lines 30-33].

As per claim 5, Arimilli discloses using a write-through core cache [*L1 cache may be*

a store-through cache; col. 10, lines 62-63].

As per claim 6, Arimilli discloses implementing a line replacement policy in said

region [*L2 controller 214 controls L1 least recently used (LRU) unit and maintains an hybrid L2 LRU*

232; Fig. 4; col. 10, lines 20-30].

As per claim 8, Arimilli discloses handling a core cache miss by passing the

details of the access to said region [*if load operation in L1 results in a miss, the load address is*

piped out to lower level storage (L2) subsystem; col. 8, lines 43-49].

As per claim 11, Arimilli discloses an article comprising a medium storing

instructions [*L1 instruction cache 254*; Fig. 5] that enable a processor based system to

define a multilevel cache [*e.g., L1 and L2*; col. 8, lines 19-21] including a core having

relatively faster components [*L1 cache is faster since it is closest to processor core*; col. 8, lines

19-21; col. 9, lines 47-50; *L1 cache is composed of high-speed components;* col. 2, lines 34-46];

and a region including relatively slower components [*directory of the lower level (L2) cache, L2*

cache is slower than L1 cache; col. 5, line 32; *L2 cache can store a much larger amount of information*

and encounters a longer access penalty than the L1 cache; col. 2, lines 34-46]; and managing the

core from said region [*upper level cache in the core is updated by searching lower level cache*

directory; col. 5, lines 30-33].

As per claim 12, Arimilli discloses managing the core from a level 2 cache [*upper*

level cache in the core is updated by searching lower level (L2) cache directory; col. 5, lines 30-33].

As per claim 15, Arimilli discloses using a write-through core cache [*L1 cache may*

be a store-through cache; col. 10, lines 62-63].

As per claim 16, Arimilli discloses implementing a line replacement policy in said

region [*L2 controller 214 controls L1 least recently used (LRU) unit and maintains an hybrid L2 LRU

232*; Fig. 4; col. 10, lines 20-30].

As per claim 18, Arimilli discloses handling a core cache miss by passing the

details of the access to said region [*if load operation in L1 results in a miss, the load address is

piped out to lower level storage (L2) subsystem*; col. 8, lines 43-49].

As per claim 21, Arimilli discloses a processor [*CPU 150*; Fig. 3]; a multilevel

cache [*e.g., L1 and L2*; col. 8, lines 19-21] including a core having relatively faster

components [*L1 cache is faster since it is closest to processor core*; col. 8, lines 19-21; col. 9,

lines 47-50]; and a region including relatively slower components [*directory of the lower level

(L2) cache, L2 cache is slower than L1 cache*; col. 5, line 32]; and a storage coupled to said

processor storing instructions [*L1 instruction cache 254*; Fig. 5] that enable the processor to

manage the core from said region [*upper level cache in the core is updated by searching lower

level cache directory*; col. 5, lines 30-33].

As per claim 22, Arimilli discloses managing the core from a level 2 cache [*upper

level cache in the core is updated by searching lower level (L2) cache directory*; col. 5, lines 30-33].

As per claim 25, Arimilli discloses using a write-through core cache [*L1 cache may

be a store-through cache*; col. 10, lines 62-63].

As per claim 26, Arimilli discloses implementing a line replacement policy in said

region [*L2 controller 214 controls L1 least recently used (LRU) unit and maintains an hybrid L2 LRU

232*; Fig. 4; col. 10, lines 20-30].

As per claim 28, Arimilli discloses handling a core cache miss by passing the details of the access to said region [*if load operation in L1 results in a miss, the load address is piped out to lower level storage (L2) subsystem*; col. 8, lines 43-49].

Claim Rejections - 35 USC § 103

8.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9.   Claims 3, 4, 7, 9-10, 13, 14, 17, 19-20, 23, 24 and 27, 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US6,463,507) and Wu (US5,668,968).

As per claims 3, 13 and 23, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach using a virtual address to index the core to avoid the need for an address translation mechanism as recited in the claims.

Wu discloses using a virtual address to index the core to avoid the need for an address translation mechanism [*portion of the virtual address is used to index the L1 cache, and L1 cache uses a real pointer to point to the corresponding line in L2 cache*; col. 6, lines 52-56; lines 66-67].

As per claims 4, 14 and 24, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. Arimilli further discloses placing functions relating to valid bits in the core [*one state bit, valid/invalid is provided*; col. 10, lines 61-64]. However, Arimilli does not specifically teach placing functions relating to tags and valid bits as well as the data itself in the core as recited in the claims.

Wu discloses placing functions relating to tags as well as the data itself in the core [*the remainder of the virtual address becomes a virtual address tag stored in L1 cache directory to indicate whether the corresponding line of data is stored in L1*; col. 6, line 51 – col. 7, line 3].

As per claims 7, 17 and 27, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach performing virtual-to-physical translation in said region as recited in the claims.

Wu discloses performing virtual-to-physical translation in said region [*L2 cache is a real cache where real address are generated (e.g., virtual address are translated to real address)*; col. 10, lines 39-41; col. 6, lines 58-59].

As per claims 9, 19 and 29, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach enabling said region to use a memory translation mechanism to determine the physical address and attributes of the access [*TLB generates real address which comprises a 20-bit real page number and a 12-bit offset*; col. 10, lines 39-43].

As per claims 10, 20 and 30, Arimilli discloses the claimed invention as detailed

above in the previous paragraphs. However, Arimilli does not specifically teach

checking to see if the requested data is in a storage associated with said region as

recited in the claims.

Wu discloses checking to see if the requested data is in a storage associated

with said region [*the remainder of the real address indicates whether the corresponding line of data is*

stored in L2 cache; col. 7, lines 4-8].

It would have been obvious to one of ordinary skill in the art, having the

teachings of Arimilli and Wu before him at the time the invention was made, to modify

the system of Arimilli to include using a virtual address to index the core to avoid the

need for an address translation mechanism; placing functions relating to tags as well as

the data itself in the core; performing virtual-to-physical translation in said region;

enabling said region to use a memory translation mechanism to determine the physical

address and attributes of the access; checking to see if the requested data is in a

storage associated with said region because it would have (1) reduced the cache

coherence complexity in the system because the real, lower level cache always include

the lines in the virtual, upper level cache [col. 6, lines 40-45] and (2) modified the L1

cache with limited overhead because the needed information can be quickly accessed

[col. 6, lines 49-51] as taught by Wu.

Response to Arguments

10.   Applicant's arguments filed August 20, 2003 have been fully considered but they are not persuasive. As to the remarks, Applicant asserted that:

Arimilli fails to teach or suggest defining a multilevel cache including a core having relatively faster components and a region including relatively slower components because Arimilli makes no mention of one cache having faster components than the other.

Examiner respectfully traverses applicant's arguments for the following reasons. Examiner would like to emphasize that Arimilli does disclose a cache having faster components than the other as detailed in column 2, lines 34-46. Note that Arimilli discloses that the instruction cache 32 and the data cache 34, which both compose the L1 cache are high-speed caches as detailed in column 2, lines 34-35. Thus, it can be seen that the L1 cache is composed of high-speed components. Arimilli further discloses that the L2 cache can store a much larger amount of information and encounters a longer access penalty than the L1 cache as detailed in column 2, lines 37-40. Thus, the L2 cache components, being larger, are slower than the L1 cache components. In light of the foregoing, it can be seen that Arimilli clearly teaches that one cache has faster components than the other.

Conclusion

11.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

12.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-

5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate

Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone

number for the organization where this application or proceeding is assigned is (703)

746-7239.

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is (703) 305-

9000.

Pierre M. Vital
Art Unit 2188
January 14, 2004

Mano Padmanabhan

Supervisory Patent Examiner

TC2100